Cmos Test And Evaluation A Physical Perspective

Using the book and the software provided with it, the reader can build his/her own tester arrangement to investigate key aspects of analog-, digital- and mixed system circuits Plan of attack based on traditional testing, circuit design and circuit manufacture allows the reader to appreciate a testing regime from the point of view of all the participating interests Worked examples based on theoretical bookwork, practical experimentation and simulation exercises teach the reader how to test circuits thoroughly and effectively

Model based testing is the most powerful technique for testing hardware and software systems. Models in Hardware Testing describes the use of models at all the levels of hardware testing. The relevant fault models for nanoscaled CMOS technology are introduced, and their implications on fault simulation, automatic test pattern generation, fault diagnosis, memory testing and power aware testing are discussed. Models and the corresponding algorithms are considered with respect to the most recent state of the art, and they are put into a historical context by a concluding chapter on the use of physical fault models in fault tolerance.

Este libro contiene las presentaciones de la XVII Conferencia de Diseño de Circuitos y Sistemas Integrados celebrado en el Palacio de la Magdalena, Santander, en noviembre de 2002. Esta Conferencia ha alcanzado un alto nivel de calidad, como consecuencia de su tradición y madurez, que lo convierte en uno de los acontecimientos más importantes para los circuitos de microelectrónica y la comunidad de diseño de sistemas en el sur de Europa. Desde su origen tiene una gran contribución de Universidades españolas, aunque hoy los autores participan desde catorce países

The Electronic Device Failure Analysis Society proudly announces the Seventh Edition of the Microelectronics Failure Analysis Desk Reference, published by ASM International. The new edition will help engineers improve their ability to verify, isolate, uncover, and identify the root cause of failures. Prepared by a team of experts, this updated reference offers the latest information on advanced failure analysis tools and techniques, illustrated with numerous real-life examples. This book is geared to practicing engineers and for studies in the major area of power plant engineering. For non-metallurgists, a chapter has been devoted to the basics of material science, metallurgy of steels, heat treatment, and structure-property correlation. A chapter on materials for boiler tubes covers composition and application of different grades of steels and high temperature alloys currently in use as boiler tubes and future materials to be used in supercritical, ultra-supercritical and advanced ultra-supercritical thermal power plants. A comprehensive discussion on different mechanisms of boiler tube failure is the heart of the book. Additional chapters detailing the role of advanced material characterization techniques in failure investigation and the role of water chemistry in tube failures are key contributions to the book.

Includes bibliographical references and index.

This book constitutes the proceedings of the 6th International Conference on Nonlinear Speech Processing, NOLISP 2013, held in Mons, Belgium, in June 2013. The 27 refereed papers included in this volume were carefully reviewed and selected from 34 submissions. The paper are organized in topical sections on speech and audio analysis; speech synthesis;

speech-based biomedical applications; automatic speech recognition; and speech enhancement.

Identifying Emerging Trends in Technological Innovation Doctoral programs in science and engineering are important sources of innovative ideas and techniques that might lead to new products and technological innovation. Certainly most PhD students are not experienced researchers and are in the process of learning how to do research. Nevertheless, a number of empiric studies also show that a high number of technological innovation ideas are produced in the early careers of researchers. The combination of the eagerness to try new approaches and directions of young doctoral students with the experience and broad knowledge of their supervisors is likely to result in an important pool of innovation potential. The DoCEIS doctoral conference on Computing, Electrical and Industrial En- neering aims at creating a space for sharing and discussing ideas and results from doctoral research in these inter-related areas of engineering. Innovative ideas and hypotheses can be better enhanced when presented and discussed in an encouraging and open environment. DoCEIS aims to provide such an environment, releasing PhD students from the pressure of presenting their propositions in more formal contexts.

Transient current (iDDT) refers to the current drawn from the power supply durin g the transient switching of CMOS gates. Testing based on the transient current can detect many of the defects that can occur in ICs, such as resistive opens, w hich may not be detected by traditional voltage testing or by Leakage current (I DDQ) testing methods. A major set back for IDDQ testing methods is the increased leakage currents in today's ICs. Thus iDDT based testing has been often investi gated as an alternative or supplement to (IDDQ) testing. Little work has focused on iDDT testing for domino circuits. In this thesis, we propose a method for testing domino CMOS circuits using the transient power supp ly current. The method is based on monitoring the peak value of the transient cu rrent. This peak varies considerably with process variations, so each process ha s different thresholds; this problem will be addressed by proposing a normalizat ion procedure that allows us to use a single threshold for all processes. We pre sent also a test vector generation algorithm for testing large domino circuits. We evaluate the effectiveness of this testing method by simulation on various do mino circuits of different sizes. We develop and implement a partitioning technique to improve the fault coverage of the test method when used with large circuits. The algorithm divides the circ uit into different clusters where each cluster is fed by a different power suppl y branch. We also provide an automation system to simplify the process of genera ting the simulation files, injecting the defects in the circuit, running the sim ulations, storing the simulations output, processing the output signals, and fin ally gathering and analyzing the results.

Power supply current monitoring to detect CMOS IC defects during production testing quietly laid down its roots in the mid-1970s. Both Sandia Labs and RCA in the United States and Philips Labs in the Netherlands practiced this procedure on their CMOS ICs. At that time, this practice stemmed simply from an intuitive sense that CMOS ICs showing abnormal quiescent power supply current (IDDQ) contained defects. Later, this intuition was supported by data and analysis in the 1980s by Levi (RACD, Malaiya and Su (SUNY-Binghamton), Soden and Hawkins (Sandia Labs and the University of New Mexico), Jacomino and co-workers (Laboratoire d'Automatique de Grenoble), and Maly and co-workers (Carnegie Mellon University). Interest in IDDQ testing has advanced beyond the data reported in the 1980s and is now focused on applications and evaluations involving larger volumes of ICs that improve quality beyond what can be achieved by previous conventional means. In the conventional style of testing one attempts to propagate the logic states of the suspended nodes to primary outputs. This is done for all or most nodes of the circuit. For sequential circuits, in particular, the complexity of finding suitable tests is very high. In comparison, the IDDQ test does not observe the logic states, but measures the integrated current that leaks through all gates. In

other words, it is like measuring a patient's temperature to determine the state of health. Despite perceived advantages, during the years that followed its initial announcements, skepticism about the practicality of IDDQ testing prevailed. The idea, however, provided a great opportunity to researchers. New results on test generation, fault simulation, design for testability, built-in self-test, and diagnosis for this style of testing have since been reported. After a decade of research, we are definitely closer to practice.

The book covers the most recent developments in machine learning, signal analysis, and their applications. It covers the topics of machine intelligence such as: deep learning, soft computing approaches, support vector machines (SVMs), least square SVMs (LSSVMs) and their variants; and covers the topics of signal analysis such as: biomedical signals including electroencephalogram (EEG), magnetoencephalography (MEG), electrocardiogram (ECG) and electromyogram (EMG) as well as other signals such as speech signals, communication signals, vibration signals, image, and video. Further, it analyzes normal and abnormal categories of real-world signals, for example normal and epileptic EEG signals using numerous classification techniques. The book is envisioned for researchers and graduate students in Computer Science and Engineering, Electrical Engineering, Applied Mathematics, and Biomedical Signal Processing.

CMOS Test and Evaluation: A Physical Perspective is a single source for an integrated view of test and data analysis methodology for CMOS products, covering circuit sensitivities to MOSFET characteristics, impact of silicon technology process variability, applications of embedded test structures and sensors, product yield, and reliability over the lifetime of the product. This book also covers statistical data analysis and visualization techniques, test equipment and CMOS product specifications, and examines product behavior over its full voltage, temperature and frequency range.

Device testing represents the single largest manufacturing expense in the semiconductor industry, costing over $40 billion a year. The most comprehensive and wide ranging book of its kind, Testing of Digital Systems covers everything you need to know about this vitally important subject. Starting right from the basics, the authors take the reader through automatic test pattern generation, design for testability and built-in self-test of digital circuits before moving on to more advanced topics such as IDDQ testing, functional testing, delay fault testing, memory testing, and fault diagnosis. The book includes detailed treatment of the latest techniques including test generation for various fault models, discussion of testing techniques at different levels of integrated circuit hierarchy and a chapter on system-on-a-chip test synthesis. Written for students and engineers, it is both an excellent senior/graduate level textbook and a valuable reference.

With the evolution of semiconductor technology and global diversification of the semiconductor business, testing of semiconductor devices to systems for electrostatic discharge (ESD) and electrical overstress (EOS) has increased in importance. ESD Testing: From Components to Systems updates the reader in the new tests, test models, and techniques in the characterization of semiconductor components for ESD, EOS, and latchup. Key features: Provides understanding and knowledge of ESD models and specifications including

human body model (HBM), machine model (MM), charged device model (CDM), charged board model (CBM), cable discharge events (CDE), human metal model (HMM), IEC 61000-4-2 and IEC 61000-4-5. Discusses new testing methodologies such as transmission line pulse (TLP), to very fast transmission line pulse (VF-TLP), and future methods of long pulse TLP, to ultra-fast TLP (UF-TLP). Describes both conventional testing and new testing techniques for both chip and system level evaluation. Addresses EOS testing, electromagnetic compatibility (EMC) scanning, to current reconstruction methods. Discusses latchup characterization and testing methodologies for evaluation of semiconductor technology to product testing. ESD Testing: From Components to Systems is part of the authors' series of books on electrostatic discharge (ESD) protection; this book will be an invaluable reference for the professional semiconductor chip and system-level ESD and EOS test engineer. Semiconductor device and process development, circuit designers, quality, reliability and failure analysis engineers will also find it an essential reference. In addition, its academic treatment will appeal to both senior and graduate students with interests in semiconductor process, device physics, semiconductor testing and experimental work.

This volume contains a collection of papers presented at the NATO Advanced Study Institute on ·Testing and Diagnosis of VLSI and ULSI" held at Villa Olmo, Como (Italy) June 22 -July 3,1987. High Density technologies such as Very-Large Scale Integration (VLSI), Wafer Scale Integration (WSI) and the not-so-far promises of Ultra-Large Scale Integration (ULSI), have exasperated the problema associated with the testing and diagnosis of these devices and systema. Traditional techniques are fast becoming obsolete due to unique requirements such as limited controllability and observability, increasing execution complexity for test vector generation and high cost of fault simulation, to mention just a few. New approaches are imperative to achieve the highly sought goal of the • three months· turn around cycle time for a state-of-the-art computer chip. The importance of testing and diagnostic processes is of primary importance if costs must be kept at acceptable levels. The objective of this NATO-ASI was to present, analyze and discuss the various facets of testing and diagnosis with respect to both theory and practice. The contents of this volume reflect the diversity of approaches currently available to reduce test and diagnosis time. These approaches are described in a concise, yet clear way by renowned experts of the field. Their contributions are aimed at a wide readership: the uninitiated researcher will find the tutorial chapters very rewarding. The expert wiII be introduced to advanced techniques in a very comprehensive manner.

This book gives clear explanations of the technical aspects of electronics engineering from basic classical device formulations to the use of nanotechnology to develop efficient quantum electronic systems. As well as being up to date, this book provides a broader range of topics than found in many other electronics books. This book is written in a clear, accessible style and

covers topics in a comprehensive manner. This book's approach is strongly application-based with key mathematical techniques introduced, helpful examples used to illustrate the design procedures, and case studies provided where appropriate. By including the fundamentals as well as more advanced techniques, the author has produced an up-to-date reference that meets the requirements of electronics and communications students and professional engineers. Features Discusses formulation and classification of integrated circuits Develops a hierarchical structure of functional logic blocks to build more complex digital logic circuits Outlines the structure of transistors (bipolar, JFET, MOSFET or MOS, CMOS), their processing techniques, their arrangement forming logic gates and digital circuits, optimal pass transistor stages of buffered chain, sources and types of noise, and performance of designed circuits under noisy conditions Explains data conversion processes, choice of the converter types, and inherent errors Describes electronic properties of nanomaterials, the crystallites' size reduction effect, and the principles of nanoscale structure fabrication Outlines the principles of quantum electronics leading to the development of lasers, masers, reversible quantum gates, and circuits and applications of quantum cells and fabrication methods, including self-assembly (quantum-dot cellular automata) and tunneling (superconducting circuits), and describes quantum error-correction techniques Problems are provided at the end of each chapter to challenge the reader's understanding

This book provides a new multi-method, process-oriented approach towards speech quality assessment, which allows readers to examine the influence of speech transmission quality on a variety of perceptual and cognitive processes in human listeners. Fundamental concepts and methodologies surrounding the topic of process-oriented quality assessment are introduced and discussed. The book further describes a functional process model of human quality perception, which theoretically integrates results obtained in three experimental studies. This book's conceptual ideas, empirical findings, and theoretical interpretations should be of particular interest to researchers working in the fields of Quality and Usability Engineering, Audio Engineering, Psychoacoustics, Audiology, and Psychophysiology. Presents a new process-oriented approach towards speech quality assessment to uncover influences of speech transmission quality on human information processing; Proposes a multi-method assessment approach including subjective, behavioral, and neurophysiological levels of analysis; Reports findings from three experimental studies, that demonstrate interactions between perceived speech quality, contextual, and content-related influencing factors.

Microelectronic Test Structures for CMOS Technology and Products addresses the basic concepts of the design of test structures for incorporation within test-vehicles, scribe-lines, and CMOS products. The role of test structures in the development and monitoring of CMOS technologies and products has become ever more important with the increased cost and complexity of development and

manufacturing. In this timely volume, IBM scientists Manjul Bhushan and Mark Ketchen emphasize high speed characterization techniques for digital CMOS circuit applications and bridging between circuit performance and characteristics of MOSFETs and other circuit elements. Detailed examples are presented throughout, many of which are equally applicable to other microelectronic technologies as well. The authors' overarching goal is to provide students and technology practitioners alike a practical guide to the disciplined design and use of test structures that give unambiguous information on the parametrics and performance of digital CMOS technology.

This book treats important topics in "Acoustic Echo and Noise Control" and reports the latest developments. Methods for enhancing the quality of transmitted speech signals are gaining growing attention in universities and in industrial development laboratories. This book, written by an international team of highly qualified experts, concentrates on the modern and advanced methods.

This book presents a statistical parametric speech synthesis (SPSS) framework for developing a speech synthesis system where the desired speech is generated from the parameters of vocal tract and excitation source. Throughout the book, the authors discuss novel source modeling techniques to enhance the naturalness and overall intelligibility of the SPSS system. This book provides several important methods and models for generating the excitation source parameters for enhancing the overall quality of synthesized speech. The contents of the book are useful for both researchers and system developers. For researchers, the book is useful for knowing the current state-of-the-art excitation source models for SPSS and further refining the source models to incorporate the realistic semantics present in the text. For system developers, the book is useful to integrate the sophisticated excitation source models mentioned to the latest models of mobile/smart phones.

An efficient automatic test pattern generator for I$sb{DDQ}$ current testing of CMOS digital circuits is presented. The complete two-line bridging fault set is considered. Because of the time constraints of I$sb{DDQ}$ testing, an adaptive genetic algorithm (GA) is used to generate compact test sets. To accurately evaluate the test sets, fault grading is performed using a switch-level fault simulator and a mixed-mode electrical-level fault simulator. The test sets are compared with those generated by HITEC, a traditional gate-level test generator. Experimental results for ISCAS85 and ISCAS89 benchmark circuits are presented. The results show that for I$sb{DDQ}$ testing, the GA test sets outperform the HITEC test sets. When the test sets are truncated due to test time constraints, the fault coverages can differ by 10% or more. In addition to test generation and test evaluation, diagnosis (fault location) is also performed using both test sets. Diagnosis is performed using fault dictionaries constructed during test evaluation. In addition to the traditional full dictionary, two reduced dictionaries are also presented. The results show that the reduced dictionaries offer good size-resolution trade-offs when compared with the full dictionary.

The theme for the 2019 conference is Novel Computing Architectures. Papers will include discussions on the advent of Artificial Intelligence and the promise of quantum computing that are driving disruptive computing architectures; Neuromorphic chip designs on one hand, and Quantum Bits on the other, still in R&D, will introduce new computing circuitry and memory elements, novel materials, and different test methodologies. These novel computing architectures will require further innovation which is best achieved through a collaborative Failure Analysis community composed of chip manufacturers, tool vendors, and universities.
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Testing techniques for VLSI circuits are undergoing many exciting changes. The predominant method for testing digital circuits consists of applying a set of input stimuli to the IC and monitoring the logic levels at primary outputs. If, for one or more inputs, there is a discrepancy between the observed output and the expected output then the IC is declared to be defective. A new approach to testing digital circuits, which has come to be known as IDDQ testing, has been actively researched for the last fifteen years. In IDDQ testing, the steady state supply current, rather than the logic levels at the primary outputs, is monitored. Years of research suggests that IDDQ testing can significantly improve the quality and reliability of fabricated circuits. This has prompted many semiconductor manufacturers to adopt this testing technique, among them Philips Semiconductors, Ford Microelectronics, Intel, Texas Instruments, LSI Logic, Hewlett-Packard, SUN microsystems, Alcatel, and SGS Thomson. This increase in the use of IDDQ testing should be of interest to three groups of individuals associated with the IC business: Product Managers and Test Engineers, CAD Tool Vendors and Circuit Designers. Introduction to IDDQ Testing is designed to educate this community. The authors have summarized in one volume the main findings of more than fifteen years of research in this area.